REMARKS

In the Office Action, the Examiner indicated that claims 1-19 are pending in the application and that all of the pending claims are rejected.

General Comments on Examiner's Responsive Comments

At paragraph 6 on page 3 of the Office Action, the Examiner asserts that the applicants' argument contradicts with the disclosure. Applicants respectfully disagree with the Examiner's comment and points out the following. Applicants do not recite in the specification that "large capacitors are used and are configured to form a charge pump...". Rather, applicants correctly state that capacitors that are larger than those used for transmitting data across the capacitive interface are used in the present invention ("Although only smaller capacitors are needed for transmitting data across the capacitive interface, **larger** capacitors are used and are configured to form a charge pump to generate power to the interface at all times.") Applicants' argument does not contradict the disclosure. Indeed, the capacitors of the present invention are larger than the smaller capacitors used for transmitting data across the capacitive interface.

Rejection under 35 U.S.C. §112

On page 4 of the Office Action, the Examiner has rejected claims 1-19 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connection, to make and/or use the invention. Applicants respectfully traverse the Examiner's rejection.

With respect to the doubling of the voltage of the clock signal as recited in claims 1,

2, and 7-9, it is submitted that an analysis of Figure 2 by one of ordinary skill in the art clearly shows the diode configuration of D1, D2, and D3, and that with such a configuration, the voltage of the clock signal will be doubled. In addition, however, this doubling is specifically recited in the specification (page 7, lines 6-7 "Diodes D1, D2 and D3 rectify and double the clock signals for the purpose of charge pumping.").

The Examiner also asserts that the limitation "a maximum capacitance of 500 pF; and a minimum capacitance of 10 pF" is not supported by the disclosure. Claims 15 and 18 have been amended to recite that the capacitive element is of a capacitance sufficient to create the charge pump of the present invention. This is clearly supported by the specification.

In view of the above comments, it is respectfully submitted that claims 1-19 meet the requirements of 35 U.S.C. §112, first paragraph; accordingly, the Examiner is respectfully requested to reconsider and withdraw the rejection of claims 1-19 under 35 U.S.C. §112, first paragraph.

Rejection Under 35 U.S.C. §103

On page 5 of the Office Action, the Examiner has rejected claims 14-19 under 35 U.S.C. §103(a) as being unpatentable over the combination of Hein et al., Hershbarger et al., and Kan et al. as applied to claims 1-13 in the prior Office Action.

To support a rejection under 35 U.S.C. §103, a reason, suggestion, or motivation to lead an inventor to combine two or more references must be found. *Pro-Mold and Tool Co. v. Great Lakes Plastics Inc.*, 37 U.S.P.Q.2d 1627, 1629 (Fed.Cir. 1996). The Examiner has not met his burden in establishing a reason, suggestion, or motivation for combining the cited references, as discussed below.

The Present Invention

The present invention relates to an interface utilizing existing clock signals from a driver circuit, such as a DSP, to charge capacitors that are normally used for capacitive coupling of digital data across a high voltage isolation barrier. Using relatively small capacitors (e.g., capacitors in the range between 10 pF and 500 pF, and preferably at 100 pF) a charge pump is formed to generate power to the interface at all times. Thus, the interface always has a steady source of power available for use, including during the on-hook state, for powering circuitry that can detect, modulate, and transmit on-hook signals across the capacitive interface.

The claimed invention includes circuitry that doubles the voltage of the clock signal coming from the DSP, thereby obtaining more power for use by a data access arrangement (DAA) coupled to the interface and, therefore to the DSP. Further, the interface circuit is a fully differential circuit, thereby eliminating the need to keep the impedance across the capacitive coupling low, as is required when using a pseudo-differential interface circuit.

Hein et al., U.S. Patent No. US 6,198,816 B1

U.S. Patent No. 6,198,816 teaches a communication system utilizing a capacitive isolation barrier to linearly attenuate the tip/ring signal voltage levels from the high phone line levels to levels within integrated circuit technology limitations. The Hein isolation circuit illustrated, for example, in Fig. 13A and Fig. 13B, is a pseudo-differential circuit. For example, receiver 262 of Fig. 13b is not a differential receiver. At best, it illustrates a pseudo-differential circuit.

The capacitive isolation barrier of Hein requires very large capacitors, e.g., at least 10,000 pF. With the large capacitances required by Hein, the impedance is low with

respect to the signals across the capacitance; thus, what is done by Hein to avoid the extensive filtering that must be utilized to filter out existing common mode signals and also common mode signals generated by the interface itself if lower capacitances were used in connection with the pseudo-differential circuit.

Hershbarger et al., U.S. Patent No. 5,664,984

Hershbarger et al. teach a method and apparatus for communicating a modulated signal across an isolation barrier using capacitors, similar to the capacitive isolation barrier of Hein et al. Like Hein, Hershbarger utilizes a pseudo-differential circuit which is thus very sensitive to impedance, thereby requiring that the capacitive coupling have a high value, e.g., 10,000 pF. Hershbarger is relied upon by the Examiner for its teaching of the use of a DSP with a charge pump for high voltage isolation for a DAA.

Kan et al., U.S. Patent No. 6,020,773

Kan et al. teaches a clock signal generator for generating a plurality of clock signals with different phases.

The Claimed Invention Is Not Taught or Suggested by Hein, Hershbarger or Kan, Either Alone or in Combination

As noted above, to support a rejection under 35 U.S.C. §103, the cited references must suggest a reason, suggestion, or motivation to lead an inventor to combine two or more references must be found. None of the references cited by the Examiner teach or suggest a driver circuit, such as a charge pump, which doubles the voltage of a clock signal provided by the driver circuit to thus increase the voltage available for use by a DAA. In addition, none of Hein, Hershbarger, or Kan teach or suggest the use of a fully differential

signal processing circuit and thus require very large value capacitors and/or filtering elements if the size of the capacitors are reduced.

The claims of the present invention, as amended, positively recite these novel and distinguishing features (claim 1, "a charge pump ... doubling the voltage of said clock signal"; claim 8, "a charge pump ... doubling the voltage of said charge and passing said doubled voltage to said DAA to provide said operating power."; claim 14, "An interface circuit as set forth in claim 1, wherein said interface circuit is a fully differential circuit"; claim 15, "An interface circuit as set forth in claim 2 wherein said first capacitive element has a capacitance sufficient to create said charge pump."). Since none of these elements are taught or suggested by Hein, Hershbarger or Kan, it is submitted that the claims, as amended, patentably define over the cited references.

Applicants maintain their assertion that the claimed invention is a fully differential circuit and that the Hein circuit is a pseudo-differential circuit.

The present invention uses a differential charge pump and differential transmission circuit because of undesirable common mode voltages. The circuit of Hein will fail in the presence of a large common mode voltage. This is apparent to one of ordinary skill in the art. By contrast, the present invention rejects common mode voltages of any level, regardless of the value of the capacitors. As an example, a typical 150 volt peak-to-peak common mode voltage presented across the Hein circuit will cause it to fail, while the same 150 volt peak-to-peak voltage across the present invention will not inhibit the present invention in any way.

The present invention patentably defines over the cited references and is thus in condition for allowance. The Examiner is respectfully requested to reconsider and withdraw his rejection of the claims under 35 U.S.C. §103.

Conclusion

The claims, as amended, patentably define over the prior art cited by the Examiner in rejecting the claims. Accordingly, reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 15 and 18 have been amended as follows:

15. (Once amended) An interface circuit as set forth in claim 2, wherein said first capacitive element has a capacitance sufficient to create said charge pump[:

a maximum capacitance of 500 pF; and

a minimum capacitance of 10 pF].

18. (Once amended) An interface circuit as set forth in claim 9, wherein said first capacitive element has a capacitance sufficient to create said charge pump[:

a maximum capacitance of 500 pF; and

a minimum capacitance of 10 pF].